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Characterization of Polycrystalline Silicon Thin-Film Transistors

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The nonlinear behavior of the transfer characteristics of polycrystalline silicon thin-film transistors (poly-Si TFTs) at the threshold voltage was analyzed. The threshold voltage V_T was defined as the gate voltage giving half of the maximum transconductance ($G_{mMAX}/2$). The nonlinear parameter ΔV was also introduced as the maximum transconductance divided by the differential of G_m at V_T. V_T and ΔV increased as the density of defect states increased. Moreover, ΔV increased as the energy level of defects increased near the band edge. ΔV gave the carrier density and the Fermi level at the silicon surface at V_T. V_T and ΔV also gave the density of occupied defects states at V_T. Analysis using V_T and ΔV was applied to the characterization of n-channel TFTs fabricated with laser crystallization and H_2O vapor annealing. V_T and ΔV were 0.90 and 0.81 V, respectively. They gave the Fermi level and the densities of electron carrier and occupied defect states at the threshold voltage as 0.91 eV, 2.2×10^{10} and $1.8 \times 10^{11}\,cm^{-2}$, respectively. [DOI: 10.1143/JJAP.45.1534]

KEYWORDS: TFTs, defect states, Fermi level, transconductance

1. Introduction

Polycrystalline silicon thin-film transistors (poly-Si TFTs) have been widely developed for fabrication of electronic devices such as flat panel displays.[1–3] Low-temperature fabrication processing has been attractive because it allows us to fabricate TFTs on substrates with a low heat resistivity, such as glass or plastic.[4–7] Poly-Si TFTs, however, have electrically active defects, which trap carriers, at gate insulator/silicon interfaces and in silicon films. The defects can therefore govern the characteristics of drain current. It is important to understand the behavior of drain current as a function of defect state to apply poly-Si TFTs to electronic circuits. In transfer characteristics for most poly-Si TFTs, drain current does not increase linearly as gate voltage increased from the threshold voltage, in contrast to conventional linear transfer behavior as given by the following equation;[8]

$$I_d = \frac{W}{L} C_{ox} \mu \left(V_g - V_T - \frac{V_d}{2} \right) V_d, \qquad (1)$$

where W is the width of the channel, L is the length of the channel, C_{ox} is the gate capacitance per unit area, μ is the mobility, V_g is the gate voltage, V_T is the threshold voltage, and V_d is the drain voltage. The nonlinear characteristics result in significant drain currents below the threshold voltage. The subthreshold current is caused by occupied defect states in TFTs.

In this study, we discuss transfer characteristics at the threshold gate voltage. We propose two values of the threshold voltage V_T and the nonlinear parameter ΔV in order to characterize the nonlinear characteristics of the drain current at the threshold voltage. V_T and ΔV give the Fermi level and the densities of carrier and occupied defect states at V_T. This method with V_T and ΔV is used to analyze the nonlinear transfer characteristics of n-channel TFTs fabricated with laser crystallization and H_2O vapor heat treatment.[9]

2. TFT Fabrication

Poly-Si TFTs were fabricated using pulsed laser crystallization and defect reduction processes. Hydrogenated amorphous silicon (a-Si:H) films doped with $7 \times 10^{20}\,cm^{-3}$ phosphorus and with a thickness of 30 nm were first formed on glass substrates at 330 °C using plasma-enhanced chemical vapor deposition (PECVD). The doped films were removed at the channel region 25 μm long and 75 μm wide by etching, and they were used as dopant sources for forming source and drain regions. 25-nm-thick undoped a-Si:H films were then deposited using PECVD over the entire area. The silicon layers were crystallized at room temperature in vacuum at 3×10^{-4} Pa using a 30 ns pulsed XeCl excimer laser at $275\,mJ/cm^2$ with 50 shots. Undoped crystallized regions were used as the channel region. Source and drain regions were simultaneously formed through diffusion of phosphorus atoms into the overlaying silicon layer during laser crystallization. The melt duration of silicon during laser crystallization was shorter than 100 ns, thus the diffusion distance of the dopant atoms was at most 60 nm in liquid silicon[10] and the channel length hardly changed. Some samples were heated at 260 °C with 1.3×10^6 Pa H_2O vapor for 3 h to reduce the defects in the silicon films. The molecular beam deposition method was then used to form the gate insulator.[11] A 100-nm-thick SiO_x layer was deposited at room temperature as the gate insulator by thermal evaporation of SiO powders using Knudsen cell in oxygen radical ambient at a pressure of 1×10^{-2} Pa, which was generated by 300 W induction-coupled remote plasma equipment. Contact holes were then opened in the SiO_x layer on the source and drain regions. Gate, drain, and source electrodes were formed with Al metals. After TFT fabrication, all samples were heated at 260 °C with 1.3×10^6 Pa H_2O vapor for 3 h for defect reduction in SiO_x ands SiO_x/Si interfaces. Measurements of capacitance response with a frequency of 1 MHz as a function of gate bias voltage for Al gate metal–oxide–semiconductor (MOS) capacitors with n-type silicon revealed that H_2O vapor heat treatment oxidized the SiO_x films well and improved the specific dielectric constant, the densities of interface traps, and fixed oxide charges. They were estimated to be 4.1, $5 \times 10^{10}\,cm^{-2}\,eV^{-1}$ and $2.7 \times 10^{11}\,cm^{-2}$, respectively. The TFTs were consequently prepared by two H_2O vapor heat treatments and by one H_2O vapor heat treatment.

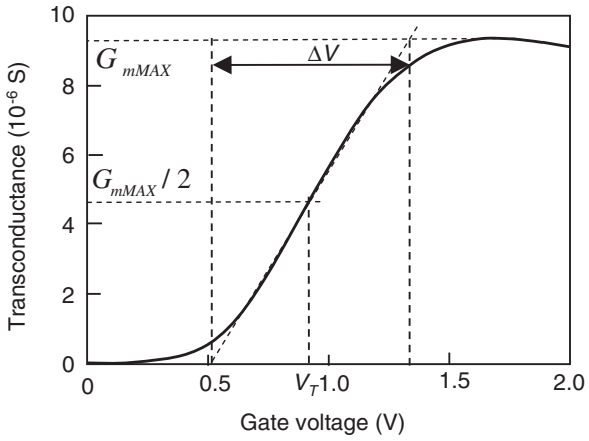

Fig. 1. Transconductance as a function of gate voltage for poly-Si TFT fabricated with H_2O vapor heat treatment applied after laser crystallization and TFT fabrication. The threshold voltage, V_T, of the drain current was defined as the gate voltage at half of the maximum transconductance, G_{mMAX}, for n-channel TFTs. ΔV was defined as the maximum transconductance divided by the increasing ratio of G_m at V_T given by the differential of G_m (see the dashed tangent line).

3. Analysis of Nonlinear Transfer Characteristics

Figure 1 shows transconductance as a function of the gate voltage for n-channel poly-Si TFTs fabricated with the H_2O vapor heat treatment applied after laser crystallization and after TFT structure fabrication. The transconductance was plotted by compensating the voltage shift so that zero gate voltage gave the flat band condition. We define the threshold voltage V_T of the drain current as the gate voltage at half of the maximum transconductance, G_{mMAX}, as shown in Fig. 1. If carrier mobility does not significantly change with gate voltage, transconductance can be given as

$$G_m(V_g) = \frac{W}{L} e\mu V_d \frac{\partial n}{\partial V_g}, \tag{2}$$

where e is the elemental charge, μ is the carrier mobility, and n is the carrier density per unit area in the channel region. When a gate voltage is applied sufficiently high to occupy defect states with electrical charges, G_{mMAX} is given approximately by the linear equation shown in eq. (1) as

$$G_{mMAX} \sim \frac{W}{L} \mu C_{ox} V_d, \tag{3}$$

The transconducatnce at the threshold voltage is therefore given as

$$G_m(V_T) = \frac{1}{2} G_{mMAX} \sim \frac{W}{2L} \mu C_{ox} V_d, \tag{4}$$

The carrier induction ratio at V_T is given by eqs. (2)–(4) as,

$$\left.\frac{\partial n}{\partial V_g}\right|_{V_g=VT} \sim \frac{1}{2}\frac{C_{ox}}{e}, \tag{5}$$

In order to characterize the nonlinear behavior of the drain current around V_T, we introduce the nonlinear parameter ΔV which is defined as the maximum transconductance divided by the increasing ratio of G_m at V_T. ΔV is given by the differential of G_m at V_T and, using eqs. (2) and (3), as

$$\begin{aligned}\Delta V &= G_{mMAX}\left(\left.\frac{\partial G_m}{\partial V_g}\right|_{V_g=VT}\right)^{-1} \\ &\sim \frac{W}{L}\mu C_{ox} V_d \left(\frac{W}{L} e\mu V_d \left.\frac{\partial^2 n}{\partial V_g^2}\right|_{V_g=VT}\right)^{-1} \\ &\sim \frac{C_{ox}}{e}\left(\left.\frac{\partial^2 n}{\partial V_g^2}\right|_{V_g=VT}\right)^{-1},\end{aligned} \tag{6}$$

ΔV means the effective gate voltage width required to increase G_m from zero to G_{mMAX}, as shown in Fig. 1. Using eqs. (5) and (6), the carrier induction ratio around V_T is approximately described by a first-order Taylor series as

$$\begin{aligned}\frac{\partial n(V_g)}{\partial V_g} &\sim \left.\frac{\partial n}{\partial V_g}\right|_{V_g=VT} + \left.\frac{\partial^2 n}{\partial V_g^2}\right|_{V_g=VT}(V_g - V_T) \\ &\sim \frac{1}{2}\frac{C_{ox}}{e} + \frac{C_{ox}}{e\Delta V}(V_g - V_T) \\ &\sim \frac{C_{ox}}{e}\left(\frac{1}{2} + \frac{V_g - V_T}{\Delta V}\right).\end{aligned} \tag{7}$$

The carrier density at V_T is therefore estimated as

$$\begin{aligned}n &\sim \int_{V_T-\Delta V/2}^{V_T} \frac{C_{ox}}{e}\left(\frac{1}{2} + \frac{V_g - V_T}{\Delta V}\right) dV_g \\ &= \frac{C_{ox}}{e}\left[\frac{\Delta V}{4} + \frac{1}{2\Delta V}\left\{V_T^2 - \left(V_T - \frac{\Delta V}{2}\right)^2\right\} - \frac{V_T}{2}\right] \\ &= \frac{C_{ox}}{8e}\Delta V.\end{aligned} \tag{8}$$

The carrier density at V_T is proportional to ΔV. The carrier density per unit area is also given by the model of the effective density of states as

$$n = N_c D \exp\left(\frac{E_F - E_G}{kT}\right), \tag{9}$$

where N_c is the effective volume density of states for the conduction band, E_G is the band gap, k is Boltzman constant, and T is the absolute temperature. D is the effective channel thickness in which carriers concentrate. Our numerical calculation program of the transfer characteristics using the finite element method combined with statistical thermodynamic conditions gave D as a function of the carrier density per unit area as $D = -2\times10^{-8}(\log n)^3 + 7\times10^{-7}(\log n)^2 - 8\times10^{-6}\log n + 3\times10^{-5}$ (cm) for the carrier density ranging from 1×10^8 to $1\times10^{12}\,\mathrm{cm}^{-2}$.[12,13] The Fermi level E_F at the gate insulator/silicon interface is given by ΔV using eqs. (8) and (9) as

$$E_F = kT \ln\frac{C_{ox}\Delta V}{8eN_c D} + E_G. \tag{10}$$

High ΔV results in a high Fermi level at the gate insulator/silicon interface at the threshold voltage.

For poly-Si TFTs, the density of charge per unit area generated in the silicon channel induced by applying gate voltage is given by charge neutralization as

$$C_{ox} V_g = e(n + N_t) \tag{11}$$

where N_t is the density of the occupied defects trapping charge per unit area. From eqs. (8) and (11), the density of

occupied defects at V_T is estimated as

$$N_t \sim \frac{C_{ox}}{e}\left(V_T - \frac{\Delta V}{8}\right). \quad (12)$$

From eqs. (5) and (11), the charge trapping ratio as a function of V_g is equal to the carrier induction ratio at the threshold voltage V_T as

$$\left.\frac{\partial n}{\partial V_g}\right|_{V_T} \sim \frac{C_{ox}}{2e} \sim \left.\frac{\partial N_t}{\partial V_g}\right|_{V_T} \quad (13)$$

The density of occupied defect states N_t at V_T is governed by the energy distribution of the density of defect states in the band gap and the Fermi–Dirac distribution at V_T. If the flat band condition is achieved at a zero gate voltage, N_t at V_T is given as the density of occupied defect states at V_T subtracted by the density of occupied defect states at the zero gate voltage as

$$N_t = \int_0^D \int_{E_V-\phi(x)}^{E_C-\phi(x)} N(\varepsilon,x)\left(\exp\left(\frac{\varepsilon - E_F(V_T)}{kT}\right)+1\right)^{-1} d\varepsilon\, dx - \int_0^D \int_{E_V}^{E_C} N(\varepsilon,x)\left(\exp\left(\frac{\varepsilon - E_F(0)}{kT}\right)+1\right)^{-1} d\varepsilon\, dx, \quad (14)$$

where D is the thickness of the silicon film, $N(\varepsilon, x)$ is the density of trap states at an energy of ε and a depth of x, E_V is the energy of the valence band edge, E_C is the energy of the conduction band edge, $\phi(x)$ is the potential change between depths of x and D, $E_F(V_T)$ is the Fermi level at V_T and at a depth of x, and $E_F(0)$ is the Fermi level under the flat band condition at a V_g of 0 V. A schematic illustration of the charge trapping ratio due to defects and the carrier induction ratio as a function of the gate voltage given by eqs. (7) and (11) is shown in Fig. 2. When the gate voltage is low and the Fermi level is far from the conduction band, the charge induced by the gate voltage is almost trapped by defects. The increasing ratio of the Fermi level with the gate voltage $\partial E_F/\partial V_g$ is low for a high density of defect states because the charge trapping ratio is limited by C_{ox}/e given by eq. (11). When the gate voltage increases near V_T, the Fermi level also increases near the conduction band edge, and the carrier induction is significant. The carrier induction ratio increases and the charge trapping ratio decreases, as shown in Fig. 2. The V_T is given by the gate voltage which gives the coincidence between the charge trapping ratio and the carrier induction ratio. The illustration shows that the carrier density at V_T is proportional to ΔV, which is given by eq. (7). ΔV strongly depends on the energy level of the defect states. When defects are near the conduction band edge, high Fermi energy is necessary in order to occupy the defect states, as shown in eq. (14). Because high Fermi energy also induces a significant carrier density, application of gate voltage simultaneously causes charge trapping and carrier induction. This causes a high transition voltage, ΔV, for the carrier induction ratio from zero to C_{ox}/e. The high-energy defect states can therefore result in serious nonlinear characteristics. As discussed above, V_T and ΔV characterize the nonlinear behavior of the drain current at the threshold voltage and give information on the Fermi level, the carrier density, and the density of occupied defects.

In order to clarify the relationship among V_T, ΔV, and defect states, numerical calculation of transfer characteristics was conducted with single-delta function like defect states that trapped carriers. The accepter-type defect states with a single energy level were spread spatially uniformly in the silicon films. V_T and ΔV were obtained by analysis of calculated transfer characteristics using eqs. (4) and (6).

Figure 3 shows ΔV as a function of V_T with different energy levels of densities of defect states per unit area at 300 K. V_T increased as the density of defect states increased for every energy level because a high gate voltage was necessary in order to occupy the defect states as shown in eqs. (11) and (12). ΔV was low when defects were located at a deep energy level at 0.6 eV. Until the defect states were half full, the Fermi level stayed below 0.6 eV, which was far from the conduction band edge. This means that the carrier density was low when the defect states located at 0.6 eV were mostly unoccupied. After the half-occupation of defect states by gate voltage sufficient application, the Fermi level increased above the energy level of the defect states. When

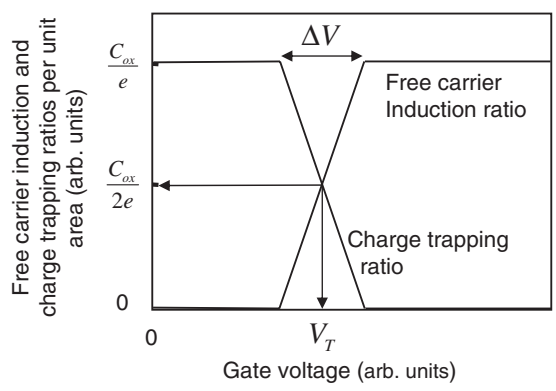

Fig. 2. Schematic illustration of changes in charge trapping ratio and carrier induction ratio with gate voltage.

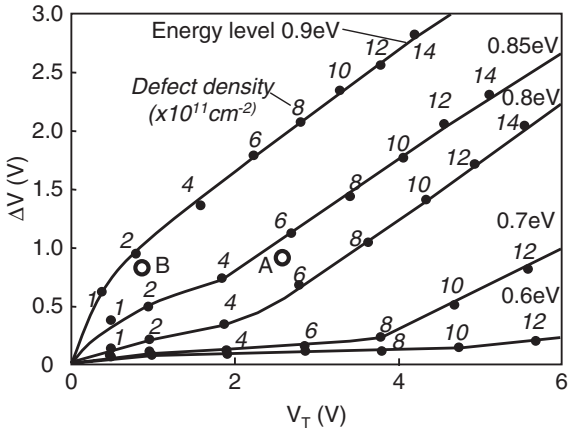

Fig. 3. ΔV as a function of V_T with different energy levels of densities of defect states per unit area at 300 K. The energy level and the density of defect states are presented in the figure. ΔV and V_T were obtained from transfer characteristics calculated using a numerical finite element program. Two data sets from ΔV and V_T were also plotted using open circles labeled A and B. They were obtained from experimental characteristics for TFTs fabricated with H_2O vapor heat treatment after only TFT fabrication (A) and for TFTs fabricated with H_2O vapor heat treatment applied after laser crystallization and after TFT fabrication (B).

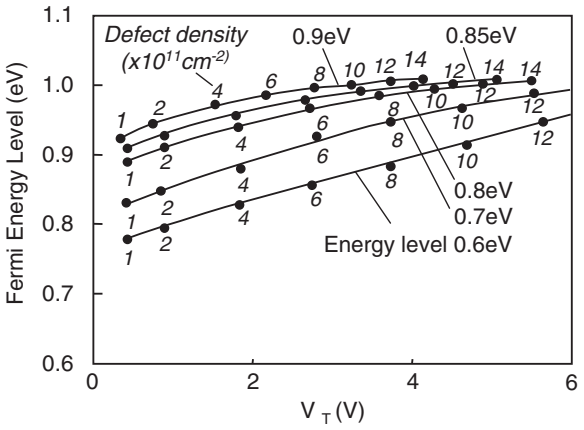

Fig. 4. Fermi level at SiO_2/Si interface as function of V_T at 300 K. The energy level and the density of defect states are presented in the figure.

the Fermi level reached an energy point which made the carrier induction ratio and the defect occupation ratio the same, V_T was determined. Figure 4 shows the Fermi level as a function of V_T at the SiO_2/Si interface at 300 K. It was 0.78 eV for defects located at 0.6 eV with a density of 1×10^{11} cm^{-2} at 300 K. The Fermi level gradually increased as V_T increased. The high density of defect states made V_T high. A high gate voltage is necessary to occupy a high density of defect states in order to achieve the charge neutrality condition given in eq. (11). The high gate voltage increased the silicon surface potential and made the potential difference between the top and bottom surfaces of the silicon layer high. This means that the Fermi level at the surface region is high at V_T. Defect states are therefore well occupied in the surface region for the case of a high density of defect states as indicated in eq. (14). The defect states at the bottom region are still unoccupied states because of the difference in the potential energy. Because defect states are gradually occupied in the depth direction as the gate voltage increases, free carriers are gradually increased. This means that ΔV increases in the case of a high density of defect states, which uniformly distribute in silicon films. V_T and ΔV therefore markedly increased with the density of defect states even for the case of deep energy levels, as shown in Fig. 4.

Figure 5 shows (a) the carrier density per unit area at V_T and (b) the density of occupied defect states per unit area at V_T as a function of the density of defect states per unit area for different energy levels of defects. Solid curves were directly estimated using eqs. (8) and (12), and dashed curves were given by numerical calculation using the finite element method. The carrier densities and the density of occupied defect states obtained by V_T and ΔV agreed with those obtained by the numerical calculation program. This means that V_T and ΔV characterize the behavior of drain current at V_T well and give the carrier density and the density of occupied defect states at V_T from experimental transfer characteristics for any energy distribution of defect states. Low V_T and low ΔV indicate low density of defect states. Low V_T and high ΔV indicate high energy level of defect states. High V_T and high ΔV indicate a high density of defect states with high energy levels.

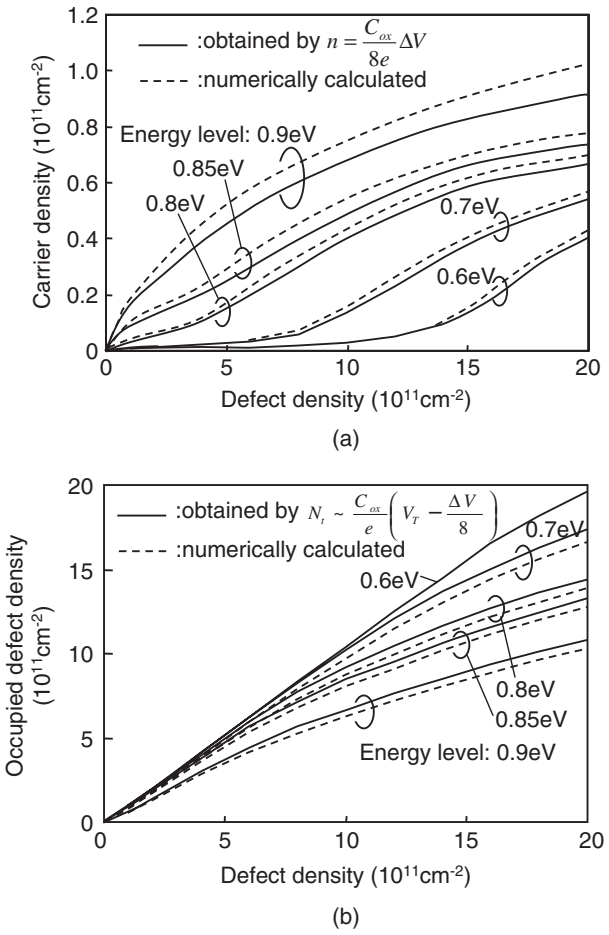

Fig. 5. (a) Carrier density per unit area at V_T and (b) the density of occupied defect states per unit area at V_T as a function of density of defect states per unit area for different energy levels of defects. Solid curves were directly calculated using eqs. (8) and (12), and dashed curves were given by numerical calculation with the finite element method.

4. Analysis of Experimental Characteristics

Figure 6 shows the transfer characteristics of TFTs (a) linear plotted and (b) plotted logarithmically. Because there was a voltage shift of -0.6 V caused by the difference in the work function between the gate metal and silicon and by the fixed oxide charge, the transfer characteristics were plotted by compensating the voltage shift so that zero gate voltage gave the flat band condition. V_T and ΔV were obtained from the transfer characteristics. They were 2.7 and 0.86 V, respectively, for TFTs fabricated with H_2O vapor heat treatment after only TFT fabrication. The V_T and ΔV gave the Fermi level, the carrier density, and the density of occupied defect states at V_T as 0.92 eV, 2.4×10^{10}, and 5.6×10^{11} cm^{-2}, respectively, according to eqs. (8), (9), and (12). On the other hand, V_T and ΔV were 0.9 and 0.81 V, respectively, for TFTs fabricated with H_2O vapor heat treatment applied after laser crystallization and TFT fabrication. The Fermi level, the carrier density, and the density of occupied defect states at V_T were estimated as 0.91 eV, 2.2×10^{10} and 1.8×10^{11} cm^{-2}, respectively. High values of ΔV for both TFTs suggest high energy level of defect states in the band gap, as shown in Fig. 3. A numerical analysis of the experimental transfer characteristics was also carried out by fitting the calculated transfer characteristics to

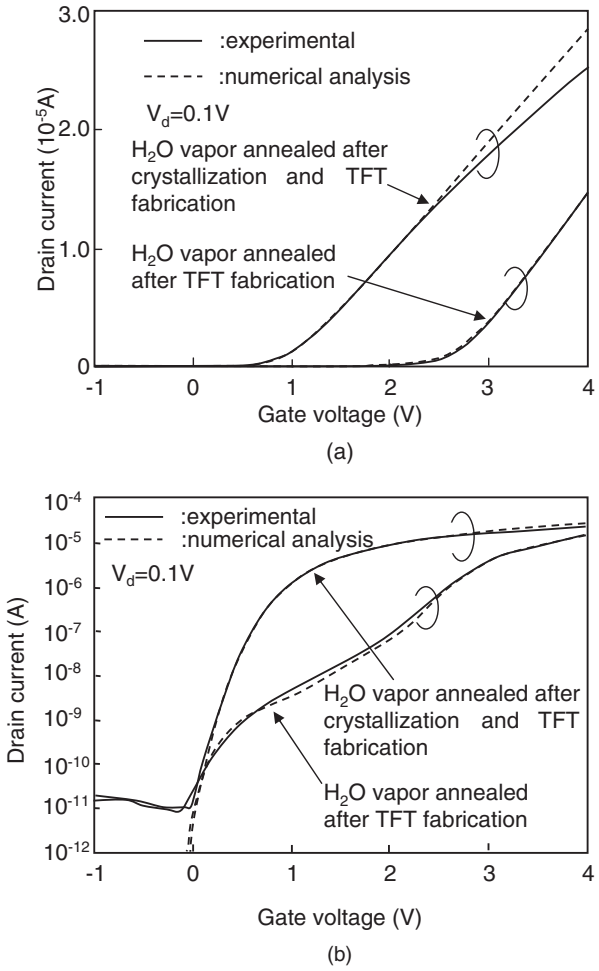

Fig. 6. Experimental and numerically calculated transfer characteristics for (a) linear plotting and (b) logarithmic plotting. Transfer characteristics were plotted under the flat band condition at zero gate voltage. TFTs were fabricated with laser crystallization at 275 mJ/cm^2 and with 1.3×10^6 Pa H_2O vapor heat treatment at 260 °C for 3 h after only TFT fabrication and with H_2O vapor heat treatment applied after laser crystallization and after TFT fabrication. Both TFTs had a W/L of 3.

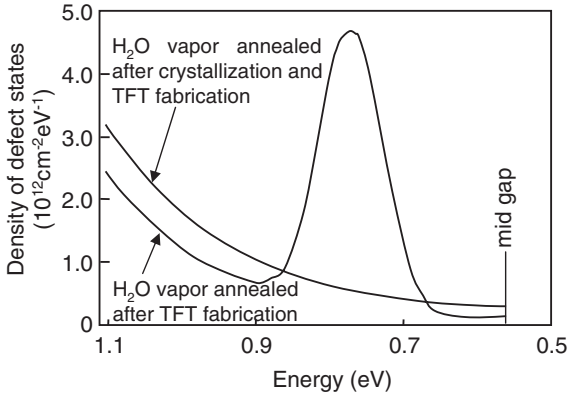

Fig. 7. Energy distribution of density of defect states obtained by fitting calculated drain current to experimental drain currents.

experimental ones as shown by dashed curves in Fig. 6. Figure 7 shows the energy distribution of the density of defect states. Both TFTs had tail-type defect states. Their density was high near the conduction band edge. The tail-type defect states essentially gave the high energy level

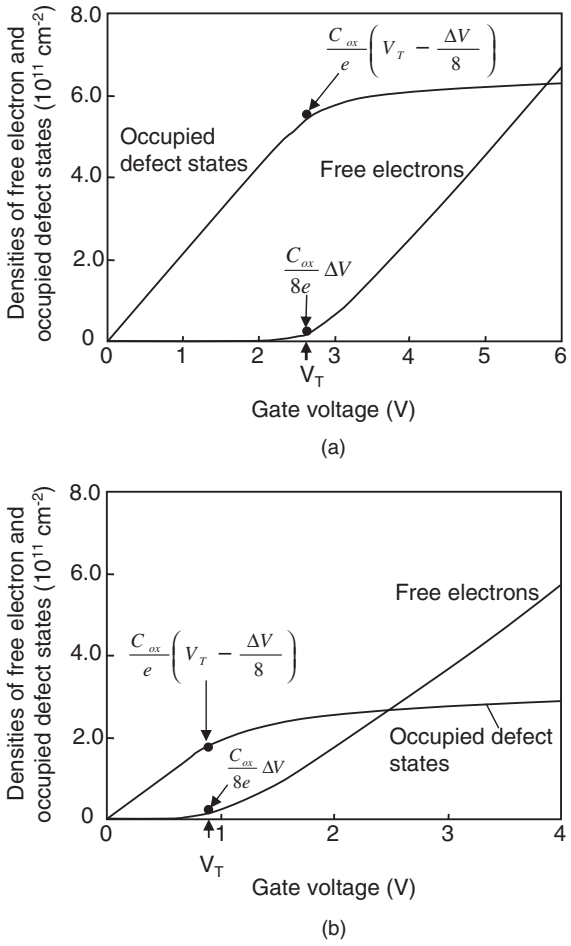

Fig. 8. Calculated densities of occupied defect states and electron carriers in silicon films as function of gate voltage (a) for TFTs fabricated with 1.3×10^6 Pa H_2O vapor heat treatment at 260 °C for 3 h only after TFT fabrication and (b) for TFTs fabricated with H_2O vapor heat treatment applied after laser crystallization and TFT fabrication.

condition, which caused the high ΔV. Moreover, a high peak of defects occurred around 0.77 eV for TFTs fabricated with H_2O vapor heat treatment after only TFT fabrication. This caused the bending of the transfer characteristics from 1.0 to 3.0 V, as shown in Fig. 6. Figure 8 shows the calculated densities of electron carriers and occupied defect states in the silicon films as a function of the gate voltage for TFTs fabricated with H_2O vapor heat treatment (a) after only TFT fabrication and (b) for TFTs fabricated with H_2O vapor heat treatment applied after laser crystallization and TFT fabrication. The densities of electron carriers and occupied defect states at V_T estimated by V_T and ΔV using eqs. (8) and (12) are also presented for both TFTs in Fig. 8. The density of occupied defect states increased almost proportionally as the gate voltage increased up to V_T. On the other hand, the density of occupied defect states gradually saturated and the carrier density increased with the gate voltage above V_T because they increased in accordance with the conditions in eq. (11). The densities of the occupied defect states and electron carriers at V_T obtained by V_T and ΔV agreed well with those given by numerical calculation, as shown in Fig. 8. The high-pressure H_2O vapor heat treatment after laser crystallization reduced the density of defect states and changed the energy distribution as shown in

Fig. 7. Both TFTs had tail states near the band edge. The tail states resulted in a high carrier trapping ratio with increased gate voltage. This caused the serious nonlinear characteristics. The high ΔV obtained from the experimental transfer characteristics of the two TFTs clearly indicates the existence of defect states near the band edge. Although the present method does not reveal the energy distribution of the density of defect states, it characterizes well the nonlinear behavior of drain current caused by defect states. ΔV and V_T simply give the Fermi level at the gate insulator/silicon interface and the densities of carriers and occupied defect states at the threshold voltage. These values are useful to analyze drain current characteristics of poly-Si TFTs.

5. Conclusions

The nonlinear behavior of transfer characteristics of poly-Si TFTs was analyzed. V_T and ΔV were introduced in order to characterize the nonlinear behavior at V_T. V_T is defined as the gate voltage giving half of the maximum transconductance ($G_{mMAX}/2$). ΔV is defined as the maximum transconductance divided by the differential of G_m at V_T. ΔV denotes the effective gate voltage width for increasing G_m from zero to G_{mMAX}. V_T and ΔV are governed by defect properties. V_T and ΔV increase as the density of defect states increases when the defect states with a single energy level are uniformly distributed in the silicon films. ΔV increases as the energy level of defect states increases near the band edge. ΔV gives the carrier density at V_T proportionally. The carrier density and the Fermi level at the silicon surface increase as the defect density and the defect energy level increase. Transfer characteristics of n-channel poly-Si TFTs were analyzed. TFTs were fabricated by XeCl excimer laser crystallization at 275 mJ/cm^2 and 100-nm-thick SiO_2 gate insulator. V_T and ΔV are 2.7 and 0.86 V, respectively, for H_2O vapor annealing after only TFT fabrication. V_T and ΔV gave the Fermi level, the densities of carriers and occupied defect states at V_T as 0.92 eV, 2.4×10^{10} and 5.6×10^{11} cm^{-2}, respectively. On the other hand, V_T and ΔV were 0.90 and 0.81 V, respectively, for the case of 1.3×10^6 Pa H_2O vapor annealing at 260 °C for 3 h after laser crystallization and TFT fabrication. The Fermi level, the densities of carriers, and occupied defect states at V_T were 0.91 eV, 2.2×10^{10} and 1.8×10^{11} cm^{-2}, respectively. These values for two different TFTs agreed with those obtained by precise numerical calculation.

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1) S. Uchikoga and N. Ibaraki: Thin Solid Films **383** (2001) 19.
2) S. Inoue, K. Sadao, T. Ozawa, Y. Kobashi, H. Kwai, T. Kitagawa and T. Shimoda: IEDM Tech. Dig., 2000, p. 197.
3) K. Shibata and H. Takahashi: Proc Int. Workshop on Active Matrix Liquid Crystal Displays'01, 2001, p. 219.
4) T. Sameshima, S. Usui and M. Sekiya: IEEE Electron Device Lett. **7** (1986) 276.
5) K. Sera, F. Okumura, H. Uchida, S. Itoh, S. Kaneko and K. Hotta: IEEE Trans. Electron Devices **36** (1989) 2868.
6) A. Kohno, T. Sameshima, N. Sano, M. Sekiya and M. Hara: IEEE Trans. Electron Devices **42** (1995) 251.
7) S. Inoue, K. Sadao, M. Matsuo, T. Hashizume, H. Ishiguro, T. Nakazawa and H. Oshima: IEDM Tech. Dig., 1991, p. 555.
8) M. B. Barron: Solid-State Electron. **15** (1972) 293.
9) T. Sameshima and M. Satoh: Jpn. J. Appl. Phys. **36** (1997) L687.
10) T. Sameshima, M. Hara and S. Usui: Mater. Res. Soc. Symp. Proc. **158** (1990) 255.
11) T. Sameshima, A. Kohno, M. Sekiya, M. Hara and N. Sano: Appl. Phys. Lett. **64** (1994) 1018.
12) M. Kimura, S. Inoue, T. Shimoda, S. W.-B. Tam, B. O.-K. Lui, P. Migliorato and R. Nozawa: J. Appl. Phys. **91** (2002) 3855.
13) P. V. Evans and S. F. Nelson: J. Appl. Phys. **69** (1991) 3605.