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Current Paths over Grain Boundaries in Polycrystalline Silicon Films

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Current paths over grain boundaries in polycrystalline silicon films have been analyzed using two-dimensional simulations. It is found that the current path is winding and longer than the distance between the electrodes. It is also found that the current path tends to flow perpendicular to the grain boundary and avoids the vertex of the grains. The reason why the current path tends to flow perpendicular to the grain boundary can also be explained using an analytical method.

KEYWORDS: current path, grain boundary, polycrystalline silicon, film, simulation, winding, perpendicularity

There has been much research analyzing carrier transport over grain boundaries in polycrystalline silicon (poly-Si) films and poly-Si thin-film transistors (TFTs).[1–25] In some research, only the axis parallel to the poly-Si layer and along the carrier transport was considered. In other research, the axis along the poly-Si depth direction was additionally considered such that carriers are induced by the vertical voltage. The other axis parallel to the poly-Si layer and perpendicular to the carrier transport is hardly considered because of the immaturity of the analytical method and the insufficiency of the computation power for three-dimensional simulations. However, in the actual devices, the carrier transport may have components along the two axes parallel to the poly-Si layer. Therefore, the objective of this paper is to analyze current paths in these two axes parallel to the poly-Si layer.

Current paths are analyzed using two-dimensional simulations. Figures 1 and 2 show the current paths in the poly-Si film for grain sizes of 0.1 μm and 1 μm, respectively. The two axes parallel to the poly-Si layer are considered, but the axis along the poly-Si depth direction is not. Therefore, carriers cannot be induced by the vertical voltage. Instead, dopants are implanted in the poly-Si film, whose density is $1.0 \times 10^{17}\,\mathrm{cm}^{-3}$. In other words, since the dopants are implanted, the three-dimensional actual devices can be reduced to two-dimensional simulations. Grains are modeled using tiled rectangles, and grain boundaries are located between the grains. The grain boundary is assumed to be a surface with trap states, whose density is $1.0 \times 10^{12}\,\mathrm{cm}^{-2}$. The trap states not only trap and reduce the carriers, but also form a potential barrier and interfere with the carrier movement. It has been confirmed that the grain boundary with trap states and working of the grain boundary are valid.[22–24] Two electrodes are located at the right and left ends of the poly-Si film, and an electric field is applied. The Poisson equation is utilized for the potential distribution, and the drift-diffusion model is utilized for the carrier transport.

From Figs. 1 and 2, it is found that the current path has components along the two axes parallel to the poly-Si layer. As a result, the current path is winding.[25,26] Therefore, the current path is longer than the distance between the electrodes. For example, as seen in Fig. 1, the current path is 110% as long as the distance between the electrodes. From Figs. 1 and 2, it is also found that the current path tends to flow perpendicular to the grain boundary. Figure 3 shows the histogram of the angle of the current path over the grain boundary for a grain size of 0.1 μm. Here, many configurations between the directions of the grain and electric field are integrated. It is confirmed that the current path tends to flow perpendicular to the grain boundary. Moreover, as evident in Figs. 1 and 2, it is also found that the current path avoids the vertex of the grains, where multiple grain boundaries encounter and form higher potential barriers. These re-

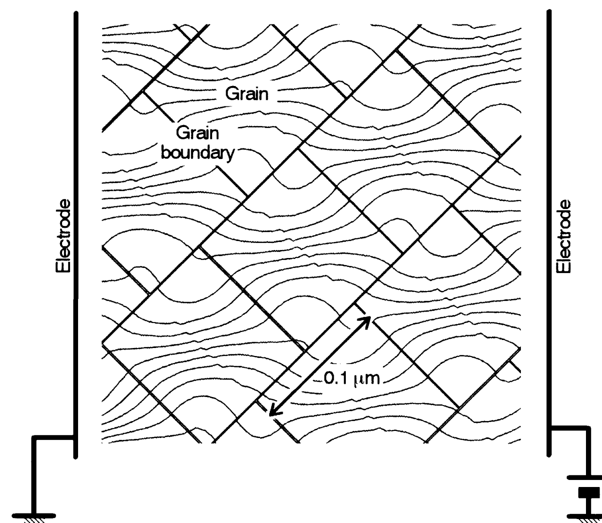

Fig. 1. Current paths in the poly-Si film for a grain size of 0.1 μm.

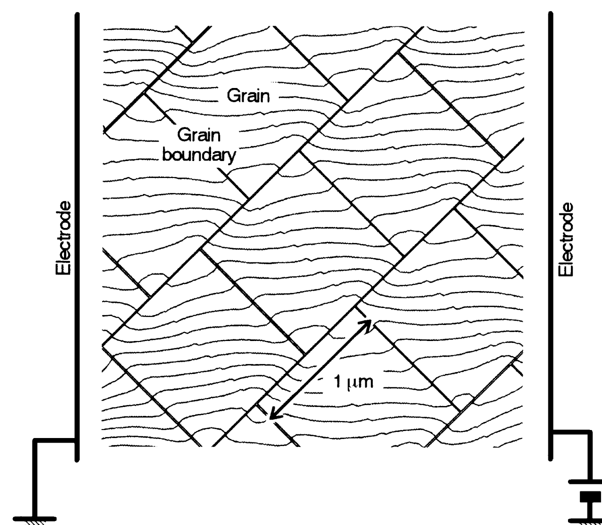

Fig. 2. Current paths in the poly-Si film for a grain size of 1 μm.

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sults are particularly conspicuous for the smaller grain size, lower dopant density and higher defect density because the potential barrier formed by the trap states at the grain boundary is more easily extended to the middle of the grain.

The reason why the current path tends to flow perpendicular to the grain boundary can also be explained using an analytical method. Figure 4 shows the current path over the grain boundary. The x-axis and y-axis are perpendicular and parallel to the grain boundary, respectively. From the drift-diffusion model, the following equation is acquired.[27)]

$$\boldsymbol{i} = q\mu n \nabla E_{\mathrm{F}} \quad (1)$$

Here, $\boldsymbol{i}$, q, μ, n and E_{F} are the current density vector, elementary electric charge, mobility, carrier density and Fermi level, respectively. The trap states at the grain boundary trap the carriers and reduce the carrier density in the neighboring grains. The carrier density recovers with distance from the grain boundary. Therefore, on the left-hand side of the grain boundary, $\partial n/\partial x < 0$. Because of the structural symmetry, $\partial n/\partial y = 0$. Because of the current continuity, $\partial i_x/\partial x = 0$, and because of the structural symmetry, $\partial i_x/\partial y = 0$. Using eq. (1) and these relationships, the following equations are acquired.

$$(\partial/\partial x)(\partial E_{\mathrm{F}}/\partial x) = [1/(q\mu n)](\partial i_x/\partial x) - (1/n)(\partial n/\partial x)(\partial E_{\mathrm{F}}/\partial x) = -[1/(q\mu n^2)](\partial n/\partial x)i_x > 0 \quad (2)$$

$$(\partial/\partial x)(\partial E_{\mathrm{F}}/\partial y) = (\partial/\partial y)(\partial E_{\mathrm{F}}/\partial x) = [1/(q\mu n)](\partial i_x/\partial y) = 0 \quad (3)$$

From eqs. (2) and (3), it is found that the gradient of the Fermi level perpendicular to the grain boundary is steeper near the grain boundary. From eq. (1), it is found that the current path is more perpendicular to the grain boundary near the grain boundary. On the right-hand side of the grain boundary, a similar explanation can be achieved.

From these results, the following conclusions are acquired. First, the current path is longer than the distance between the electrodes in the poly-Si films or the gate length in the poly-Si TFTs. This phenomenon has to be considered when the electrical characteristics are estimated. For example, when the carrier mobility is estimated from experimental results using the distance between the electrodes, this phenomenon is transferred to the carrier mobility, and the carrier mobility is underestimated. Presently, there seems to be no method for simultaneously and correctly estimating the current path and carrier mobility only from experimental results. Second, in prior research analyzing carrier transport over grain boundaries, the carrier transport was assumed to be perpendicular to the grain boundary.[1–25)] It is confirmed that this assumption is valid, and therefore the results are reliable. Third, in prior research analyzing oxide-silicon interface roughness in poly-Si TFTs, only the peak roughness was analyzed, which appeared at the vertex of the grains.[28–34)] Since the current path avoids the vertex of the grains, not only the peak roughness but also the roughness between the vertex of the grains has to be analyzed when the electrical characteristics are estimated.

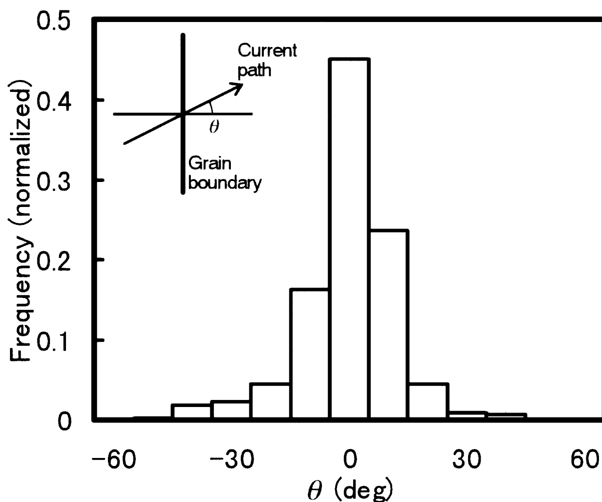

Fig. 3. Histogram of the angle of the current path over the grain boundary for a grain size of 0.1 μm.

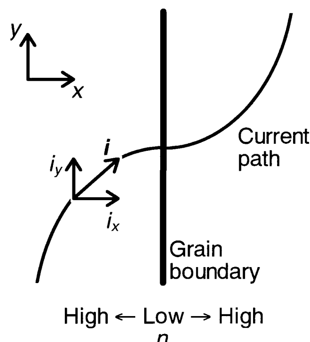

Fig. 4. Current path over the grain boundary.

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