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Section 17. Thin film transistors

Status of Si thin film transistors

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Abstract

This paper reviews fabrication processes of poly-Si thin film transistors (TFT) at a low temperature ($< 450°C$), whose technologies appeared in the nineteen-eighties and which was expected to be a new process for device applications. Pulsed laser crystallization has been developed for formation of crystalline silicon films at a low processing temperature. Although high quality poly-Si films with a high carrier mobility have been achieved by that method, there are still problems for production of TFTs. This paper also discusses the insulator/Si interface formation, which is an essential point for obtaining high performance TFTs at a low temperature. A good insulator/Si interface is achieved by the formation of insulator layers without damage or a post annealing for reduction of defects.

Keywords: TFT; Insulator; Poly-Si

1. Introduction

There has been the big progresses in technologies of thin film transistors (TFTs) and the application of TFTs to electronic devices these two decades [1–3]. The fabrication technology of amorphous silicon (a-Si) TFTs has been established. We have enjoyed laptop computers with large and flat display panels, in which a-Si TFTs are operated to address display elements. Although a-Si TFTs drive small electrical currents because of a low carrier mobility, they have a very high impedance in the 'off' state. These characteristics are suitable as switching transistors for liquid crystal display (LCD) elements. The combination of the switching a-Si TFTs with crystalline silicon driver integrated circuits (IC) has been recognized as one of the best solutions of production of large TFT–LCD panels with a high yield. On the other hand, polycrystalline silicon thin film transistors (poly-Si TFTs) have been applied to fabrication of driver IC as well as switching transistors for display panel with a small size [4]. They have been also applied to fabrication static random access memory (SRAM) as load transistors [5]. The established process uses solid phase grain growth at 600 to 1000°C for formation of polycrystalline films [6] and thermal oxidation at $\sim 1000°C$ for gate insulators [7,8]. These high temperature methods are mature and reliable for production of TFTs with a good performance. Recently, attention has been paid to fabrication of poly-Si TFTs at a low temperature because many people believe that the low temperature process overcomes problems a-Si TFTs and poly-Si TFTs fabricated with a high temperature have [9]. The low temperature fabrication process gives a possibility of formation of poly-Si TFTs with a good performance on inexpensive substrates with a size as large as substrates used for a-Si TFT–LCD.

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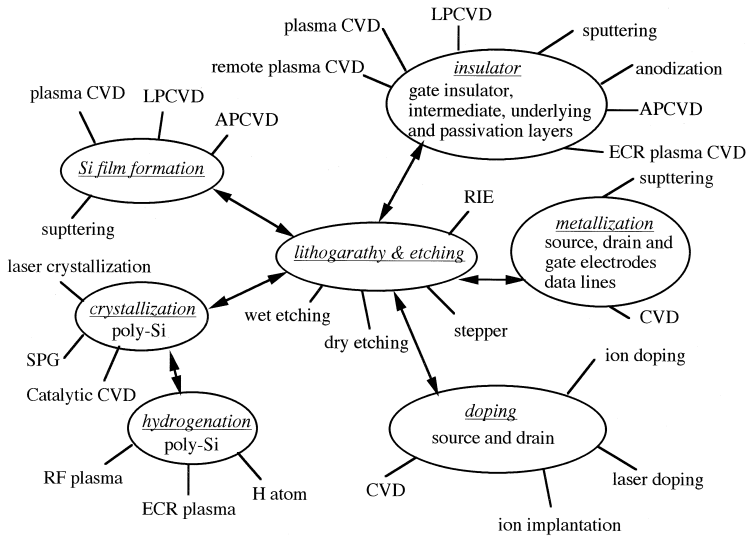

Fig. 1. Process steps and methods for their treatments for fabrication of poly-Si TFTs at a low temperature.

Electrical circuits with a high operation speed will be fabricated on plastic as well as glass substrates. Many processing steps are required for fabrication of poly-Si TFTs, as shown in Fig. 1. The processing temperature must be kept low throughout the process steps. In order to overcome this problem, many technologies have been reported. This paper reviews important points of the low temperature fabrication process for poly-Si TFTs. Then, we discuss problems on TFTs' technology to be solved.

2. Polycrystalline film formation

The pulsed excimer laser heating method has been developed to make crystalline silicon films at a low processing temperature [10–12]. Crystallization of silicon films and activation of dopant species are achieved by the laser irradiation with a small energy because of the rapid heating only the surface region to a high temperature and the liquid–solid phase change. The silicon surface region is melted and the liquid/solid interface is formed in silicon films formed on glass substrates when the silicon films are irradiated with a laser whose energy is above the melting threshold, which is 160 mJ/cm^2 if the pulse width is 30 ns [13]. The required energy for melting silicon films is quite low because the region heated by the irradiation is limited to near surface region because of a short heat diffusion length in the case of the glass substrate. Crystallization occurs along the liquid/solid interface as it moves to the surface after irradiation through heat diffusion into the substrate at the speed of the interface ~ 1 m/s [13] at a cooling rate $< 10^9$ K/s. Although the crystallization occurs very rapidly, the grain size is small (< 100 nm) because the melt duration is very short, ~ 100 ns, due to the small laser energy irradiation. We have recently investigated crystalline properties of phosphorus doped laser crystallized polycrystalline silicon films with an analysis of free carrier optical absorption, which occurred via excitation by the electrical field caused by incident photons followed by energy relaxation in the crystalline grains and Hall effect measurements [14,15]. The analysis of the free carrier absorption has given a high carrier mobility for the films formed by a low laser energy (near crystallization threshold). The mobility increases as the temperature decreases from 473 K to 77 K because of reduction of the carrier scattering by the lattice vibration as in single crystal silicon. On the other hand, the carrier mobility obtained by the Hall effect measurements decreases as the temperature decreases. The degree of the mobility reduction with temperature decreases as the laser energy increases. These results show that the crystalline grain

is formed at any laser energy, but grain boundary properties are improved by irradiation at larger laser energies. The density of the defect states could be reduced during the irradiation process with a high laser energy. Kohyama et al. has reported from their calculation that some grain boundaries can have no dangling bond (for example, $\Sigma = 9$ {122} with a rotational angle of 38.94°) so that the density of localized states and the energy barrier height can be quite low for those grain boundaries [16]. Moreover, poly-Si TFTs fabricated with laser crystallization have a similar dependence of the inversion-layer mobility on the normal electrical field to that of single crystalline metal-oxide-semiconductor-field-effect transistors (MOSFETs) [17]. Shirai and Seikawa have reported that the temperature dependence of the drain current is also similar to that of single crystalline MOSFET [18]. These calculated and experimental results may indicate that poly-Si formed by laser-induced melt-regrowth can have a grain boundary with a low energy barrier height, and that the carriers can go across that boundaries with a large effective mobility.

Large grain growth (> 1 μm) to the lateral direction is still attractive for single crystalline TFTs. Kuriyama et al. have made crystalline films with large grains (111) oriented using several laser pulses with a heated substrate (~ 400°C) [19]. Im and Kim have reported a rapid lateral grain growth by a single pulse irradiation with an energy just below the amorphization threshold energy without heating the substrate [20]. Ishihara et al. have increased lateral grain growth by reducing heat diffusion in the vertical direction using the double pulse irradiation [21]. These may be useful techniques for fabricating TFTs which have no grain boundary in the channel region.

Laser crystallization has a problem of uniformity of crystalline properties because there is an energy distribution in the beam. Pulsed laser has also an energy fluctuation pulse to pulse. Multiple pulse irradiation is required to form crystalline films uniformly over a large area at present.

Other methods have been developed for formation of poly-Si films. Metal (for example Ni)–Si reaction reduced crystallization temperature to 500°C in solid phase grain growth and TFTs have been successfully fabricated [22]. Catalytic dissociation of SiH_4 gas using hot W wire results in fabrication of poly-Si films at 300°C. A mobility of ~ 20 cm^2/Vs were reported [23].

3. SiO_2/Si interface

Formation of insulator/Si interface is an essential requirement for fabricating good TFTs with a low threshold voltage. Deposition of the gate insulator with low damage is quite important because defect reduction via thermal relaxation is not allowed in the low temperature process. Normal radio-frequency-induced plasma has ions and electrons with high energies 20 to 200 eV, which can cause damage in silicon. There are several good methods for SiO_2 formation. Serikawa et al. have reported a good SiO_2 formation at a temperature ~ 200°C using a sputtering method with O_2 gas and fabrication of poly-Si TFTs with a mobility of 380 cm^2/Vs [24]. Kim et al. have reported SiO_2 formation with a low density of interface states $\sim 10^{10}$ cm^{-2} eV^{-1} using remote plasma chemical vapor deposition (CVD) below 300°C [25]. Electron cyclotron resonance CVD gives an SiO_2 film formation with small ion damage because of a low ion energy (~ 20 eV) [26]. Thermal CVD are also attractive because plasma is not necessary but a rather high temperature, 450 to 600°C, is required for gas reaction.

We have achieved formation of the SiO_2/Si interface with a minimum trapping density of 2×10^{10} cm^{-2} eV^{-1} using remote plasma CVD with mesh electrodes to confine plasma at ~ 300°C [27,28]. The n-channel TFTs fabricated with the SiO_2 gate insulators formed by remote plasma CVD had a threshold voltage of 1 V. These results show that the reduction of plasma damage results in the improvement of the SiO_2/Si interface properties.

4. Post annealing process

A post annealing process is important for improving reliability in TFT fabrication. Hydrogenation has been widely applied to improvement of SiO_2/poly-Si interface [29–36]. Hydrogen atoms effectively terminate dangling bonds so that the threshold voltage is reduced and the carrier mobility is increased.

We have proposed a simple heating treatment in wet atmosphere (H_2O partial pressure ~ 100 Torr)

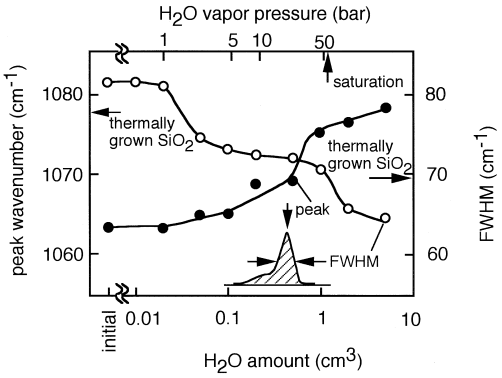

Fig. 2. The peak wavenumber of SiO optical absorption band associated with the antisymmetric stretching vibration mode and the full width at half maximum (FWHM) of the band as function of the H_2O amount (the H_2O vapor pressure) for the SiO_2 film formed by plasma CVD. The solid curves are a guide to eye. The temperature of the treatment is 270°C. The H_2O vapor pressure is estimated from the volume of the chamber and the H_2O amount put in the chamber. H_2O has the saturation pressure of 54 bar at 270°C. The error of the pressure is 2 bar, which is mainly caused by the temperature variation.

for improvement electrical properties of SiO_2 and SiO_2/Si interfaces [37]. The heating treatment effectively reduces the density of the positive charge trapped states and reduced the flat-band voltage as well as the threshold voltage. Poly-Si TFTs with a low threshold voltage have been achieved by the treatment. In general, bulk properties of SiO_2 films formed at a low temperature are not in complete thermal relaxed state [38]. The films can contain Si–O–H bonding and weak Si–O bonding with a small Si–O–Si bonding angle, which can result in an appreciable density of positive charge trapped states, a leakage current and a low break-down voltage. A heating treatment with high pressure H_2O vapor up to 54 bar at 270°C improves properties of SiO_2 and SiO_2/Si interfaces formed by plasma CVD [39]. The treatment reduced the fixed oxide charge density from 2.5×10^{12} cm^{-2} (initial) to 8×10^{10} cm^{-2} with a saturation H_2O vapor pressure of 54 bar for an Al-gate MOS capacitor. The frequency of the absorption band caused by the Si–O antisymmetric stretching mode vibration increased to 1078 cm^{-1} after treatment with a 54 bar H_2O vapor, whereas it was 1062 cm^{-1} initially, as shown in Fig. 2. The full width at half maximum (FWHM) of the absorption band was reduced from 81 cm^{-1} to 65 cm^{-1}. The density of the Si–O–H bonds was also reduced. These results indicate that this treatment makes Si–O bonding networks similar to thermally relaxed states of thermally grown oxide films. The simple heating treatment in wet atmosphere will be useful for formation of good SiO_2 and SiO_2/Si interface at a low temperature.

5. TFT fabrication equipment

Development of equipment is one of important points for fabrication of good TFTs. In-line-type and cluster-type multiple-chamber plasma CVD equipments have realized the fabrication of a-Si TFTs with high performances and a high fabrication yield. For fabrication of poly-Si TFTs, we have proposed a cluster type multiple-chamber equipment, in which laser crystallization and plasma hydrogenation and SiO_2 formation are carried out [11]. Undoped and doped silicon films are crystallized with laser irradiation in vacuum. The plasma hydrogenation is carried out to reduce defects in crystallized silicon just after crystallization. The system can keep samples clean and prevent formation of a native-oxide layer. Then SiO_2 is deposited on the silicon films as a gate insulator using remote plasma chemical vapor deposition. The 270°C process using the apparatus shown in Fig. 3 realized the fabrication of TFTs with the maximum field effect mobility, 640 cm^2/Vs for n-channel and 400 cm^2/Vs for p-channel, respectively. Moreover, the equipment allowed us to fabri-

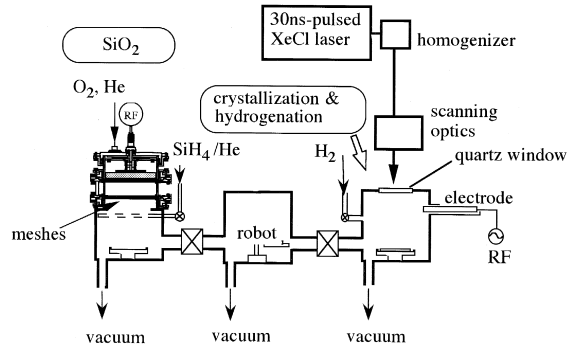

Fig. 3. Schematic of fabrication apparatus containing multiple chambers for laser irradiation, plasma hydrogenation and remote plasma CVD.

cate TFTs with uniform characteristics. The variation of the threshold voltage was ± 0.4 V in the 4-in. samples.

6. Problems in TFT processing

The substrate size in fabrication processing has been getting larger especially for a-Si TFT device. Substrates with a size of 550 mm $\times$ 650 mm are used at present. Although many devices can be fabricated from each substrate if it is large, fabrication equipment must be large and expensive. Lithography is a serious problem for large substrates. It is difficult to fabricate small TFTs with a fine design rule on a large substrate. Because of the large mobility, it is possible to fabricate electrical circuits with a high operation speed using small poly-Si TFTs. Although usage of inexpensive and large substrate is one of advantages for low-temperature fabrication process, the lithography step might limit the application.

Transfer technology would be an advantage of TFT fabrication. If TFTs or its circuits are easily removed from the substrate, on which they are fabricated, and transferred to a new substrate, the new substrate is free from the TFT fabrication process. Using the method, TFT circuits could be fabricated even on flexible organic films. TFT circuits with a high packing density could be fabricated with a very fine and precise design rule if a conventional semiconductor process is used on small substrate (< 8 in.). They can be operated on a large substrate if they are transferred on it. We have demonstrated a transfer of films by laser ablation technology. The transfer of Al and SiO_2 films is successfully carried out when an amorphous silicon layer underlays the films [40]. The a-Si film is heated rapidly by excimer laser irradiation and Al and SiO_2 films are removed.

The carrier mobility is still important for a-Si TFTs as well as poly-Si TFTs. A high carrier mobility makes rapid operation with a high current and simplification of the structure of electrical circuits possible. A high carrier mobility ~ 10 cm^2/Vs has been recently reported for a-Si films [41,42]. A rapid operation is suitable for LCD with many addressing lines and gives a possibility of fabrication of driver circuits with a-Si TFTs monolithically [43].

7. Summary

This paper reviewed some important points for fabrication processing of poly-Si TFTs at a low temperature. Pulsed laser induced heating has given a rapid crystallization of silicon films with a low laser energy at a low processing temperature. Good crystalline properties with a high carrier mobility have been achieved. There are however still problems on uniformity and reproducibility in crystallization. Catalytic CVD and solid phase grain growth are interesting for formation of poly-Si films. Gate insulator formation with a low damage is also essential for the low temperature processing. There have been already good methods of sputtering, electron cyclotron resonance plasma CVD, remote plasma CVD and thermal CVD. We have further proposed a simple annealing method with wet atmosphere to improve SiO_2 properties and SiO_2/poly-Si interfaces. Success in a-Si TFTs fabrication makes us recognize that equipment for fabrication is important. An integrated equipment, in which some process steps, crystallization, hydrogenation or SiO_2 formation can be carried out, should be developed to achieve poly-Si TFTs with a high yield. A transfer of TFT circuits into a substrate would be useful for poly-Si TFT application because the guest substrate is free from TFT fabrication process. TFTs fabricated even with the high temperature process could be operated on plastic or organic films. A high carrier mobility (~ 600 cm^2/Vs) has been achieved for poly-Si TFTs. The increase of the carrier mobility has been also reported for a-Si TFTs. It allows us to have a new idea of integrated electrical circuits.

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